ECE 6332 Design Review 1

SRAM with Sleep Cells

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A. GOAL : Make an analysis of the costs and benefits of the different designs of using sleep cells on SRAM.

B. Using Terms: Dual Supply Voltages, Dual Threshold Voltages, switching and leakage power dissipation.

C. Proposed scheme :

The approach we are thinking of is designing an SRAM with sleep cells. We will repeat the design using different locations and sizes of the sleep cells which will enable us to perform an analysis of the benefits and costs of each design.

The simulation will be done through cadence and the designs will be taken from various papers

D. Summaries of Prior Publications

1. **Ruchir Puri et al., "Pushing ASIC performance in a power envelope," in *Proceedings of the 40th annual Design Automation Conference* (Anaheim, CA, USA: ACM, 2003), 788-793.**

In this paper, it is explained the trade-off between multiple supply voltages and multiple threshold voltages on dynamic and static power optimization. Fine-grained generic voltage islands technology for multiple voltages was implemented. The clock skew scheduling as optimization techniques is discussed.

2. **Zongjian Chen et al., "A 2× load/store pipe for a low-power 1-GHz embedded processor," *Solid-State Circuits, IEEE Journal of* 38, no. 11 (2003): 1857-1865.**

In this paper, twice clocked frequency of the processor core is used on the load and store pipelines. It is called a double-pumped load and store pipe. The data cache design, which is placed the way-selection MUX before the SA, reduce the power consumption due to the minimized activating data arrays.

3. **N.S. Kim et al., "Leakage current: Moore's law meets static power," *Computer* 36, no. 12 (2003): 68-75.**

In this paper, the reduced voltages cause low power consumption, but smaller geometries like 100 nanometers, would make more energy leakage. Therefore, in terms of static power, retention flip-flops, controlling memory leakage, and compiler techniques are discussed. In addition, new technology trends, such as multiple threshold voltages, gate length, and oxide tunneling are explained.

4. **Y. Shimazaki, R. Zlatanovici, and B. Nikolic, "A shared-well dual-supply-voltage 64-bit ALU," *Solid-State Circuits, IEEE Journal of* 39, no. 3 (2004): 494-500.**

   In this paper, 64-bit arithmetic logic unit is implemented by using dual supply voltages technique. A shared n-well layout technique is used in this technique. It is accomplished to save 23% of energy compared to a conventional radix-4 full tree adder.

5. **Kyeong-Sik Min et al., "Leakage-suppressed clock-gating circuit with Zigzag Super Cut-off CMOS (ZSCCMOS) for leakage-dominant sub-70-nm and sub-1-V-VDD LSIs," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* 14, no. 4 (2006): 430-435.**

   In this paper, in order to reduce the wake-up energy consumption, the zigzag technique as sleep transistor is introduced. Using this technique, the switching and leakage energy consumption is improved. Virtual VDD line and VSS line are used to implement ZSCCMOS.

6. **J. C. Park and V. J. Mooney III, "Sleepy Stack Leakage Reduction," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* 14, no. 11 (2006): 1250-1263.**

   In this paper, the mixing techniques which combine sleep transistor and stack transistor as prior approached techniques are used. Even though they use forced stack technique, the sleepy stack technique is able to employ high threshold voltage transistors without delay overhead.

7. **Leakage control with efficient use of transistor stacks in single threshold CMOS. M. Johnson, D. Somasekhar, L.-Y. Chiou, K. Roy. IEEE Transactions on VLSI Systems, February 2002.**

   This paper try to harvest and prevent some leakage current from the fact that sometimes leakage current depends on the state of the circuit. So this paper tries to figure out what is the minimum leakage current state of the circuit and depending on the input vector, it places sleep cells in specific locations.

   The paper focuses more on how to find the input vectors that provides the minimum leakage current rather on preventing them. They came up with heuristic method to locate those input vectors. In general this paper doesn't provide much useful information other than it helps to prove that sleep cells actually reduces leakage current.

8. **A Leakage Reduction Methodology for Distributed MTCMOS. B. H. Calhoun, F. A. Honore. IEEE JSC, 2004**

   The paper focuses on multi threshold CMOS circuits that already use sleep cells on large blocks. The paper describe methods how to implement the sleeper cells on local circuits.

The main benefits come from preventing sneak leakage currents. To gain the benefits of locally implemented sleep cells, identifying the places where the sneak leakage is happening must be done. This prevented most circuit designers from using the local sleep cells. In this paper they present a methodology of locating those currents to identify the right places to add sleep cells locally.

The paper discusses the benefits and the complications of having local sleep cells. It provides a special flip-flop that would go to sleep mode depending on feedback from the output. This enables the circuit to go to sleep mode more often. Sneak leakage path is a path between Vdd and low Vt transistor or any small impedance components that are linked to ground. This contributes to big amount of leakage current to be bunt for no use.

9. **Sleep Transistor Sizing Using Timing Criticality and Temporal Currents", Proc. Asia South Pacific Design Automation Conference (ASPDAC), to appear, Jan. 2005.**

   This paper is concerned with sizing of the sleeper transistor. Other papers usually size the sleep transistor depending on the maximum worst case switching current to prevent performance penalty.

   This paper tries to estimate the size of the sleep transistor by making use of the timing criticality and the temporal switching current of the circuit. It also provides a way to accurately estimate the temporal switching current. The results have achieved good reduction in area used by the sleeper cells (50%-80%)